Exploring the Limits of ArF Lithography

Janice Golda
Assistant Director, Litho Capital Equipment Development
Intel Corporation

intel

DNS Lithography Breakfast Forum
15 July 2003

Outline

- ArF Today in Logic
- Litho requirements
  – How long can ArF meet these?
- Summary

ArF Today in Logic

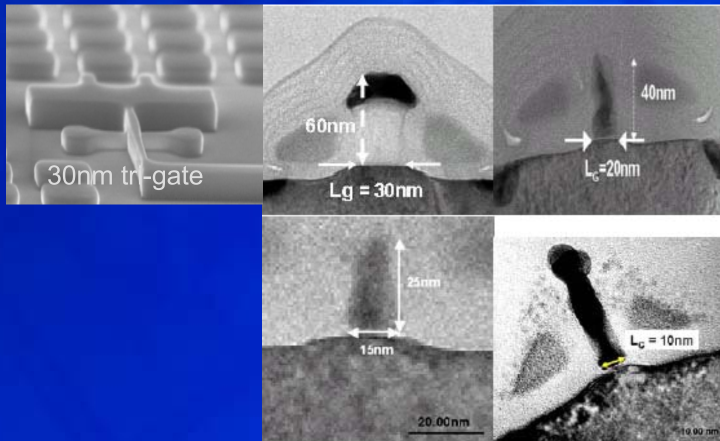
Node Name	90nm	65nm	45nm	32nm
1st Production	2003	2005	2007	2009
Logic Half Pitch	110nm	105nm	~75nm	~52nm
Gate Length	<50nm	<35nm	<25nm	~15nm
Wafer (mm)	300	300	300	300

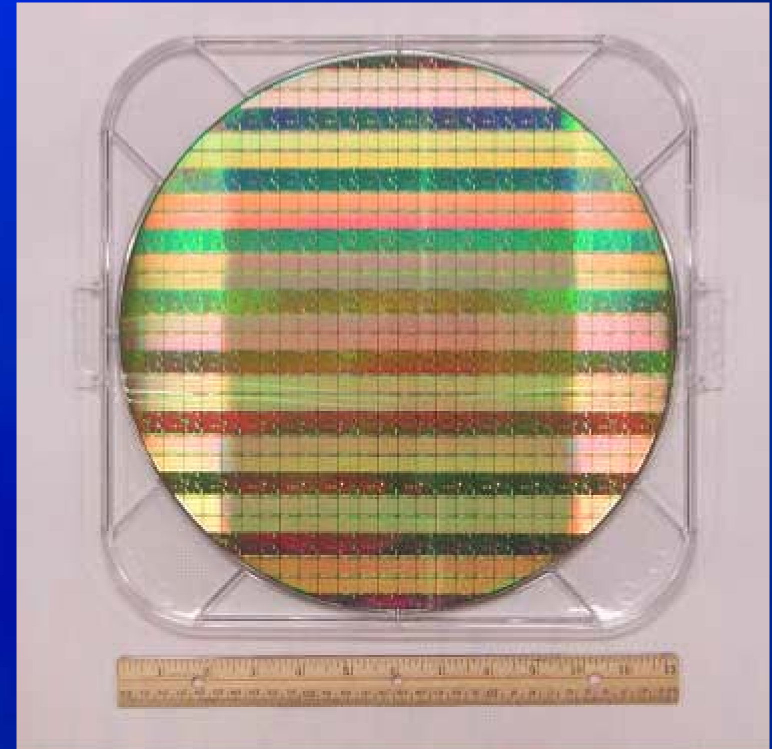
≥0.75NA ArF is ramping into 90nm 300mm production

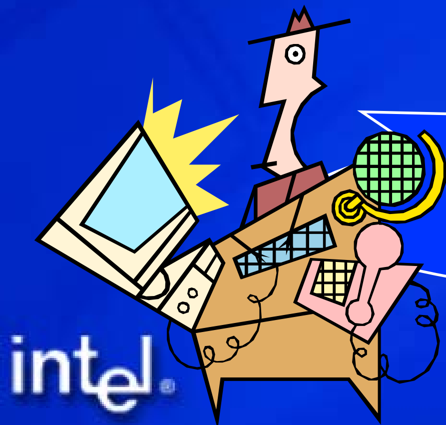
≥0.9NA ArF will begin 45nm development in '05

0.85NA ArF is supporting 65nm development

Lithography's Role: Kinko's







These transistors are good through 2013…
I just need billions of perfect copies!

Lithography Requirements

① Maintain a two year technology cycle ➜ Competition

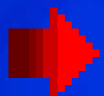
② Scale density by ~2.0X per generation ➜ Cost

③ Scale gates by ~0.6X per generation ➜ Speed

④ Flawlessly ramp new technologies into high volume

⑤ Keep lithography Affordable

➡ **What is the practical limit of ArF in logic?**



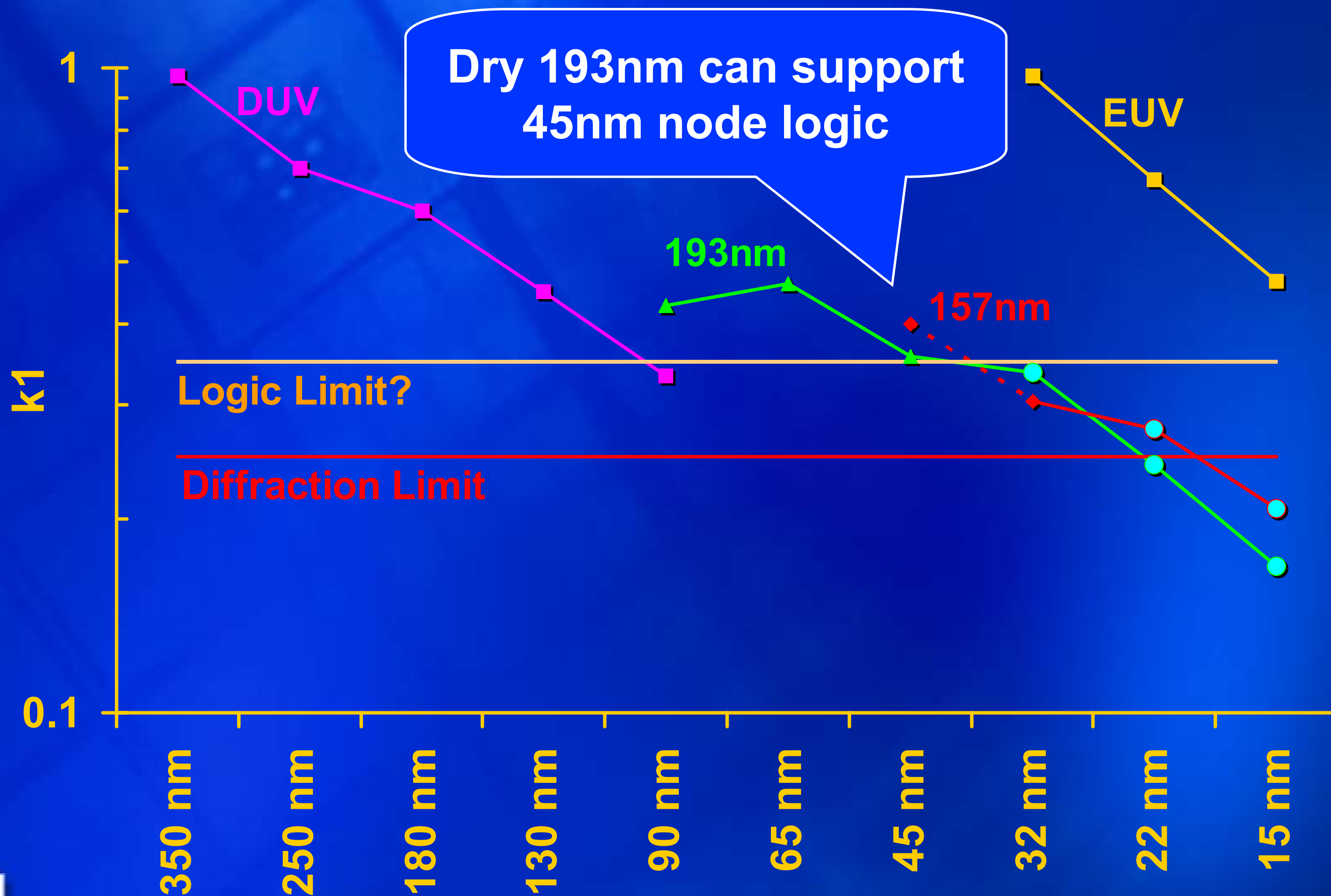
Tool Requirements

	TD Tools	Production First Tools	Production Ramp
65nm	Q1'03	Q4'03	Q4'04
45nm	Q1'05	Q4'05	Q4'06
32nm	mid'06	Q4'07	Q4'08

- TD tools support litho and testchip development
  - Same NA as production tools; may have lower run rate
- Production tools must support high volume
  - "Copy Exactly" volume deliveries
  - Affordable: 95% availability, high run rate, CoO, lifetime

intel

Scaling Limits



intel

Low k1 Patterning Challenges

- Complex, expensive masks
  - OPC + PSM
- Run rate
  - Multiple exposure
- Layout constraints
  - Polarization effects
  - Strong RETs
- Immersion feasibility
  - Defects
  - Run rate
- Process capability yield

- λ migration occurs when the cost/complexity of the new technology becomes preferable to that of the incumbent

intel

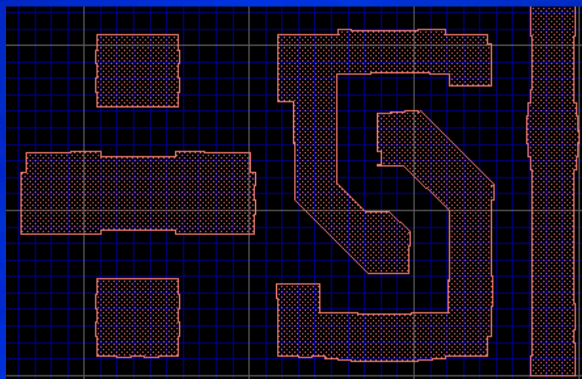
Estimated Relative Mask Costs

	Key Attributes	EUV cost relative to optical	
Mask blank	flat/defect free	similar specs	1.0
Multilayers	multilayer coated	more layers	1.2
Defect inspection	DUV inspection	similar/phase	1.2
Writing time	ebeam, similar CDs	less complex	0.5 – 0.8
Pattern Insp.	DUV inspection	less complex	0.6 – 0.8

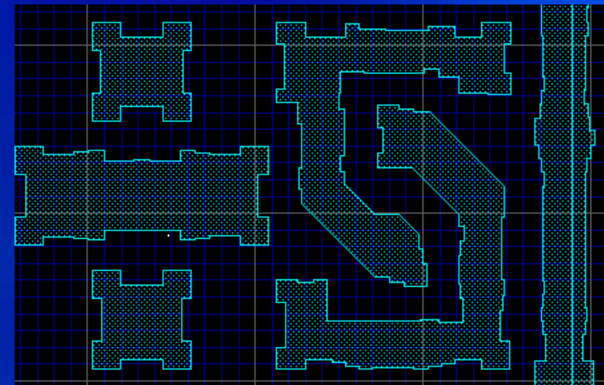
Estimated costs for 45 nm (equivalent process maturity)

Optical - OPC only	$ 100 k
OPC + complementary	$ 150 k
EUV	$ 43 - $90 k

EUV mask



Optical Mask with OPC



What is the Logic Limit of ArF?

	65nm	45nm	32nm	193nm Limits
Tool Delivery	☺	☺	?	Immersion feasibility
~2x Density	☺	😐	?	Immersion feasibility Low k1 (need 1.3NA?)
~0.6x Gate	☺	☺	?	Immersion focus + CD control
High volume	☺	😐	?	Low k1 Manufacturing Defects
Affordable	☺	☺	?	Immersion RR # PSM layers EUV readiness

intel

Summary

- **ArF will extend to support 45nm node logic**
  - Process capability will be marginal
  - ArF may extend further for memory
- **ArF has challenges to extend to 32nm**
  - Even if immersion is feasible, k1 will be low
- **EUV is the leading approach for 32nm □**
  - Focus is on commercialization